AFRL-IF-RS-TR-2005-323
In-House Final Report
September 2005

THE DESIGN AND DEVELOPMENT OF A RADIO FREQUENCY (RF) WATERMARKING SIGNATURE

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INFORMATION DIRECTORATE
ROME RESEARCH SITE
ROME, NEW YORK

Although this report references limited documents (*), listed on page 35, no limited information has been extracted.

STINFO FINAL REPORT

This report has been reviewed by the Air Force Research Laboratory, Information Directorate, Public Affairs Office (IFOIPA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

AFRL-IF-RS-TR-2005-323 has been reviewed and is approved for publication

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 074-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing this collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE SEPTEMBER 2005	3. REPORT TYPE AND DATES COVERED In-House Final, May 04 – Jun 05

4. TITLE AND SUBTITLE
THE DESIGN AND DEVELOPMENT OF A RADIO FREQUENCY (RF) WATERMARKING SIGNATURE

6. AUTHOR(S)
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5. FUNDING NUMBERS
C   - N/A
PE - 62702F
PR - 4519
TA - RF
WU - WN

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory/IFGC
525 Brooks Road
Rome New York 13441-4505

8. PERFORMING ORGANIZATION REPORT NUMBER

N/A

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Research Laboratory/IFGC
525 Brooks Road
Rome New York 13441-4505

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

AFRL-IF-RS-TR-2005-323

11. SUPPLEMENTARY NOTES

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12a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 Words)*
This report describes in-house work performed by AFRL that focused on the design and development of a Radio Frequency (RF) 'watermark signature' that can be used to authenticate a modulated signal. The objective of this effort not only included developing a watermarking technique, but also simulating it and, most importantly, using an in-house testbed to verify the technique from a hardware standpoint. Due to the subtle nature of a watermark signature, it was felt that full hardware verification was needed in order to validate the concept. A testbed comprised of field programmable gate arrays (FPGAs) and RF integrated circuits (RFICs) and were used to quickly prototype the technique.

14. SUBJECT TERMS
Radio Frequency, RF, Watermarking, Wireless, Field Programmable Gate Arrays, Simulation

15. NUMBER OF PAGES
41

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

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1. Introduction

This report will discuss research and development work performed at the Air Force Research Laboratory's Rome Research Site (AFRL-RRS). Government personnel from the Information Connectivity Branch (IFGC) performed this work in-house. The Information Connectivity Branch is concerned with, in part, wireless applications as they relate to Air Force systems.

The focus of this report is the design and development of a Radio Frequency (RF) 'watermark signature' that can be used to authenticate a modulated signal.

Most modern dictionaries define a paper watermark as "a translucent design impressed on paper during the manufacturing process and faintly visible when the paper is held at a particular angle in light". The key word here is *faintly*. Our definition of an RF watermark is "an RF design signature that is impressed during the modulation process and is faintly distinguishable to the intended receiver and non-distinguishable to the unintended receiver."

This should not be confused with a digital watermark, which is a pattern of bits inserted into a digital image, audio, or video file that identifies, for example, the file's copyright information or the file's originator.

The objective of this effort not only included developing a watermarking technique, but also simulating it and, *most importantly*, using an in-house testbed to verify the technique from a hardware standpoint. Due to the subtle nature of a watermark signature, it was felt that full hardware verification was needed in order to validate the concept. In fact, this turned out to be more crucial than originally imagined; the initial RF watermarking technique had to be abandoned due to hardware implementation difficulties.

The testbed used for hardware verification was based upon two state-of-the-art technologies: field programmable gate arrays (FPGAs) [1, 2] and Radio Frequency Integrated Circuits (RFICs) [3]. Together, these two technologies allowed for a cost effective and highly flexible testbed to develop this concept.

One of the goals of this effort was to add a RF watermark to a "conventional modulation format." Other research within IFGC was looking at more complex waveforms, such a orthogonal frequency division multiplexing (OFDM) [4]. Binary phase shift keying was investigated, but, due to its simplicity, seemed to restrict watermarking possibilities. Thus, Offset Quadrature Phase Shift Keying (OQPSK) [5] was chosen due to its balance of complexity and use in many of today's communication systems.
As mentioned earlier, the original watermark concept failed during the hardware verification phase of development; this was a disappointment after a highly promising simulation phase. This first technique impressed the watermark on the RF signal's baseband amplitude structure. After understanding the limitations of the first technique, the second concept was based upon a phase technique.

2. Development Platform

2.1 System-level Simulation

Computer simulation plays a vital role in the development of any new engineering concept. In fact, there are many levels of simulation used in the design and development of new products. IFGC has a number of simulation tools available, but the one used exclusively for this project was CoWare's Signal Processing Worksystem, or SPW [6]. SPW is a powerful tool for simulating digital signal processing concepts at various levels. It is equally at home modeling a simple subsystem as it is modeling a very complex communication system which may include transmitter, channel, and receiver.
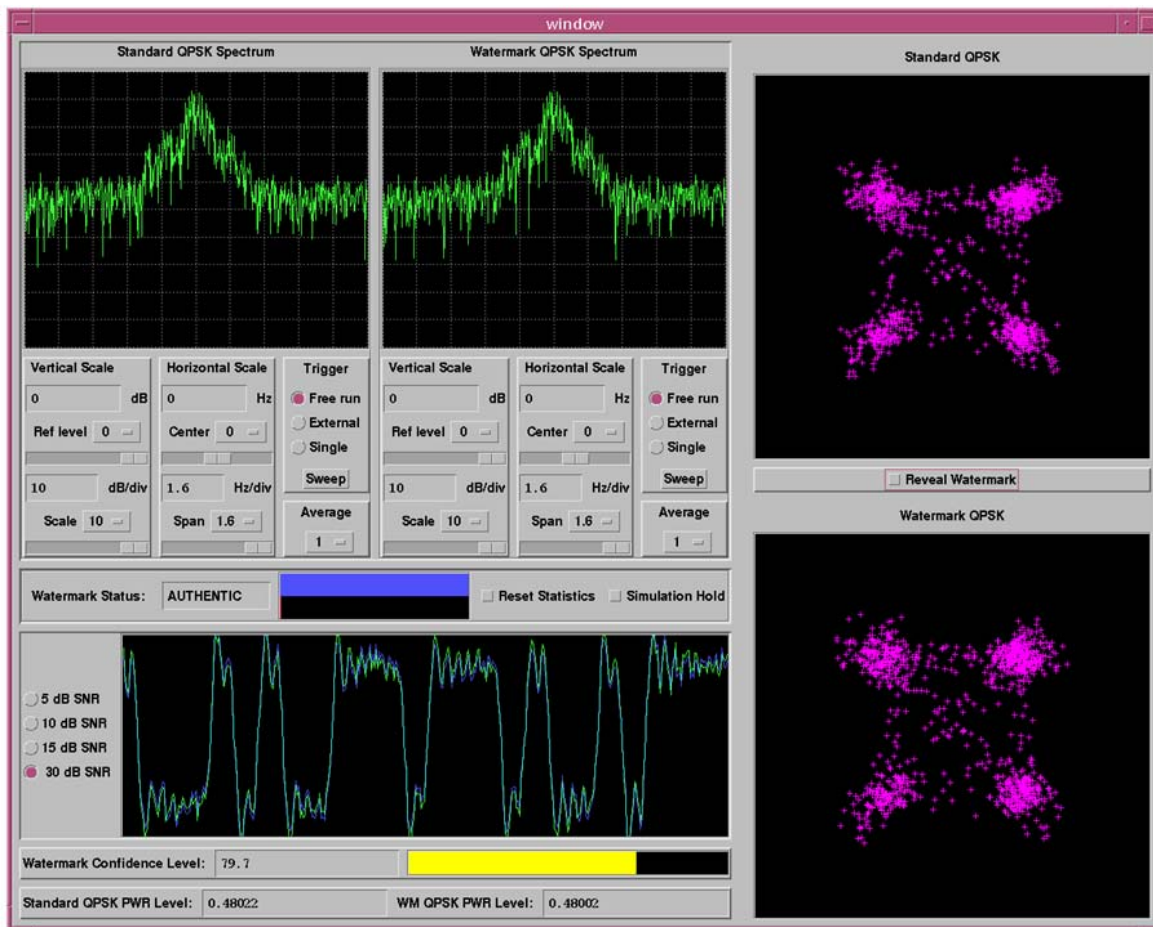

Figure 2.1-1: SPW Watermark Simulation.

This GUI is part of a simulation developed to test the first watermark signature. This amplitude-based technique passed the simulation phase of development but failed the hardware validation phase.

As with many simulation tools, SPW uses double precision floating point numbering system for simulations; but, it also has the ability to model fixed-point numbering systems. Fixed-point numbering systems are used in many of today's digital devices, such as Application Specific Integrated Circuits (ASICs) and FPGAs. SPW can also generate Hardware Description Language (HDL) code from its fixed–point models. HDL code is used by synthesis tools to create the logic used within ASICs and FPGAs.

The SPW simulation environment contains many 'virtual' instruments such as logic analyzers, oscilloscopes, waveform viewers, logic analyzer, etc. An interactive simulation was developed to test and compare a standard communications waveform with a watermarked waveform, and can be seen the figure 2.1-1. The simulation system shown in this figure was actually developed for the first watermark concept that was based upon an 'amplitude' technique. Because this technique failed the hardware phase of development, the second technique was initiated and developed at that point; bypassing the simulation phase. In general, though, all concepts begin with extensive simulation and modeling.

2.2 FPGA Software Development

IFGC's FPGA testbed was successfully developed under a previous in-house effort [7]. The design flow developed under that effort, and used for this effort, can be seen in figure 2.2-1. FPGA synthesis tools use a Hardware Description Language, such as VHDL or Verilog, in order to produce the 'logic' that will be used by the FPGA to implement one's design. As figure 2.2-1 points out, for this testbed there are two main sources which produce the HDL; namely, SPW and Xilinx's Integrated Software Environment (ISE) [1]. The important point here is that both produce the HDL code automatically from schematic diagram design tools. Writing HDL code is *rarely* needed, and mainly done for simulation testbenches.

The user creates a design using components from a library within a graphical user interface (GUI). Virtual wires, which can be single lines or buses, are used to interconnect components together. Components have inputs on the left and outputs on the right. Special symbols, referred to as I/O markers, denote inputs and outputs to the FPGA. The schematic graphical user interface of the Xilinx Engineering Capture System (ECS) can be seen in figure 3.1-3; SPW has a similar look and feel. It should be noted that this schematic may look like a circuit board layout, with several stand-alone chips being interconnected by bus and circuit traces. This is not the case; the whole design will be 'fit' into a single FPGA.

In addition to the above approaches, design components are supplemented with the Xilinx 'LogiCore' Intellectual Property (IP) modules. IP modules or 'cores', as they are often referred to, are ready-made functions that are typically much more sophisticated than standard library components. A Direct Digital Synthesizer (DDS) or a

Finite Impulse Response (FIR) filter, are two examples of IP cores used in this design. IP cores typically allow for parameter adjustment within the specific components; for example, adjusting the size of the filter, or specifying the filter coefficients.

Thus for this project, two schematic-based graphic user interfaces (SPW, ECS) along with their respective library modules, and the LogiCore IP suite, provided all the functionality necessary to implement this watermarking project.
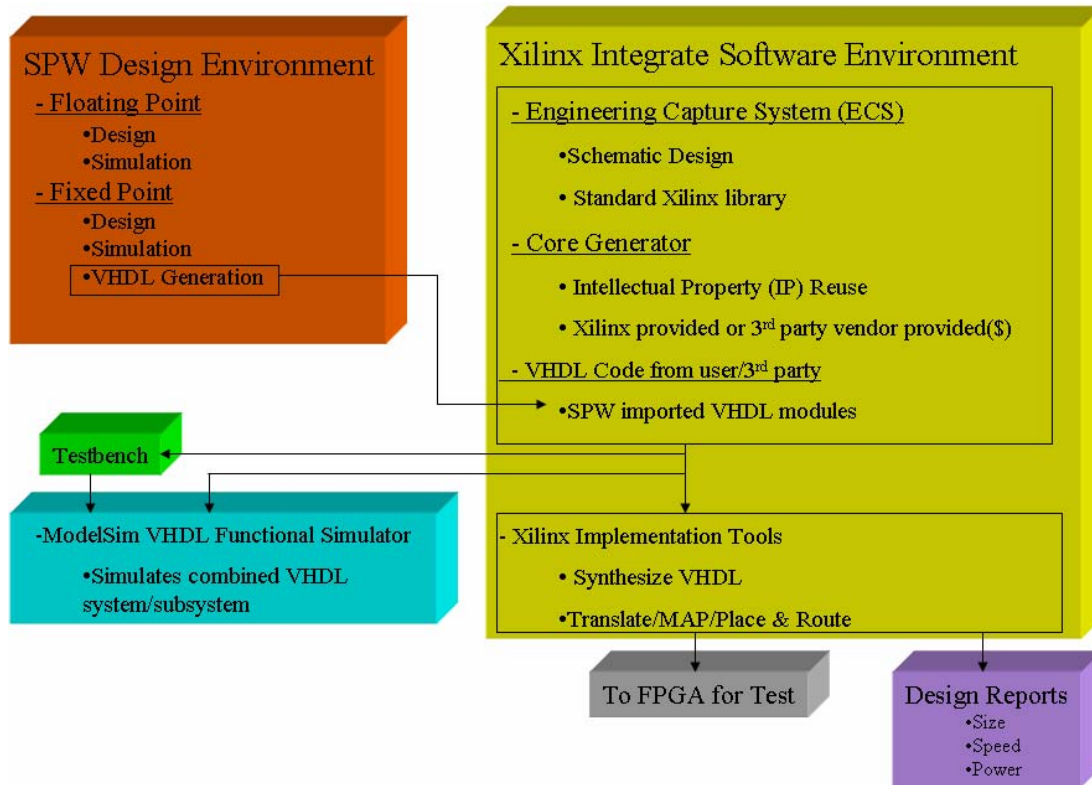

Figure 2.2-1: VHDL Design Flow.

Various software packages allow multi-level simulation of design concepts in order to verify design and assist with debug. Xilinx Integrated Software Environment truly integrates many facets of design - including 3rd party SPW developed VHDL.

2.3 FPGA Hardware

Under the pervious in-house effort [7], a specialized FPGA board was purchased from a Xilinx 'partner' company, GV & Associates, Inc [8]. The GVA-350, pictured in figure 2.3-2, is referred to as a "Virtex-II Hardware Accelerator". This stand-alone board contains the following:

- 2 Virtex-II 6000s (XV26000) FPGAs for signal processing
- 2 Spartan-II FPGAs for external interface and configuration control
- 4 channels of 100 MSPS 12-bit analog-to-digital (A/D) conversion
- 4 channels of 100 MSPS 12-bit digital-to-analog (D/A) conversion
- 512K x 18 ZBT SRAM for each XV26000
- 4 16-bit Low Voltage Differential Signaling (LVDS) headers (34-pin)
- 25-pin parallel port
- USB interface
- 8Mx8 Flash EPROM
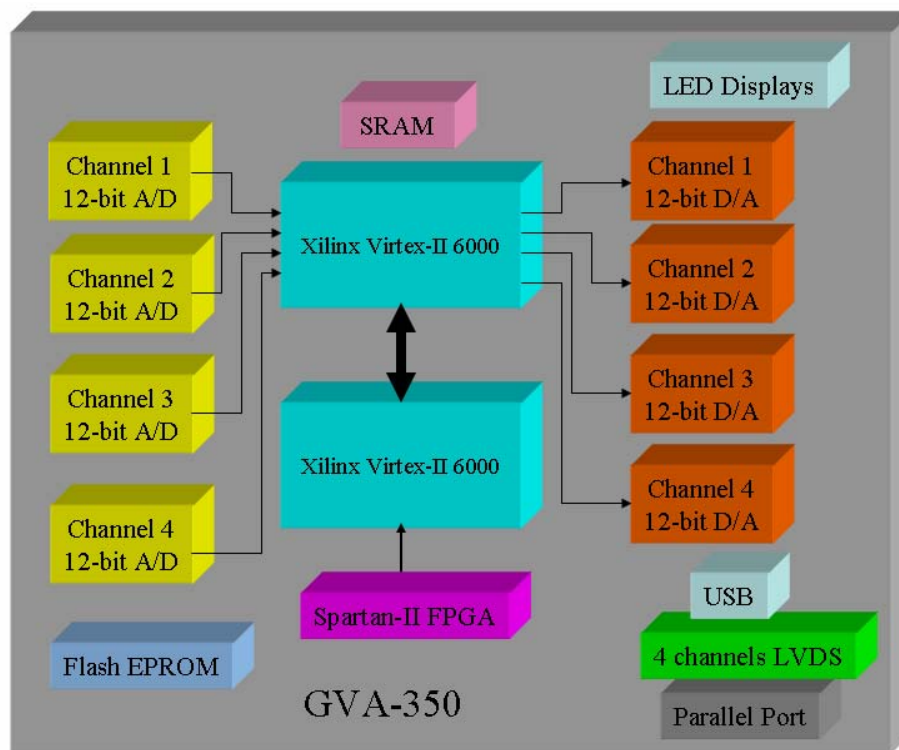- On-board 50 MHz system clock
- 2 10-bit LEDS, 4-bit DIP switch

Figure 2.3-1: GVA-350 Block Diagram.

Simplified block diagram of the GVA-350 DSP hardware accelerator. Two Virtex-II 6000s and 4 channels of A/D and D/A are ideal for prototyping various DSP algorithms involving analog signals.

The GVA-350 is a good platform for testing signal processing concepts that involve analog signals due to the fact that the board has 4 separate 100 mega sample per second (MSPS), 12-bit channels of A/D and D/A. As can be seen by the block diagram of figure 2.3-1, all eight channels are fed directly into/from one Virtex-II FPGA (referred to by the company as the 'analog' FPGA). A 203-bit bus connects this FPGA with the other

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Virtex-II (referred to as the 'digital' FPGA due to the fact that it interfaces with various ports such as USB, and LVDS). Also on board are several smaller Xilinx Spartan XC2S100 FPGAs; one of which was used for the watermark transmitter. The watermark receiver utilizes the Virtex-II 6000 which is directly connected to the analog portion of the board. This is displayed on the following figure.
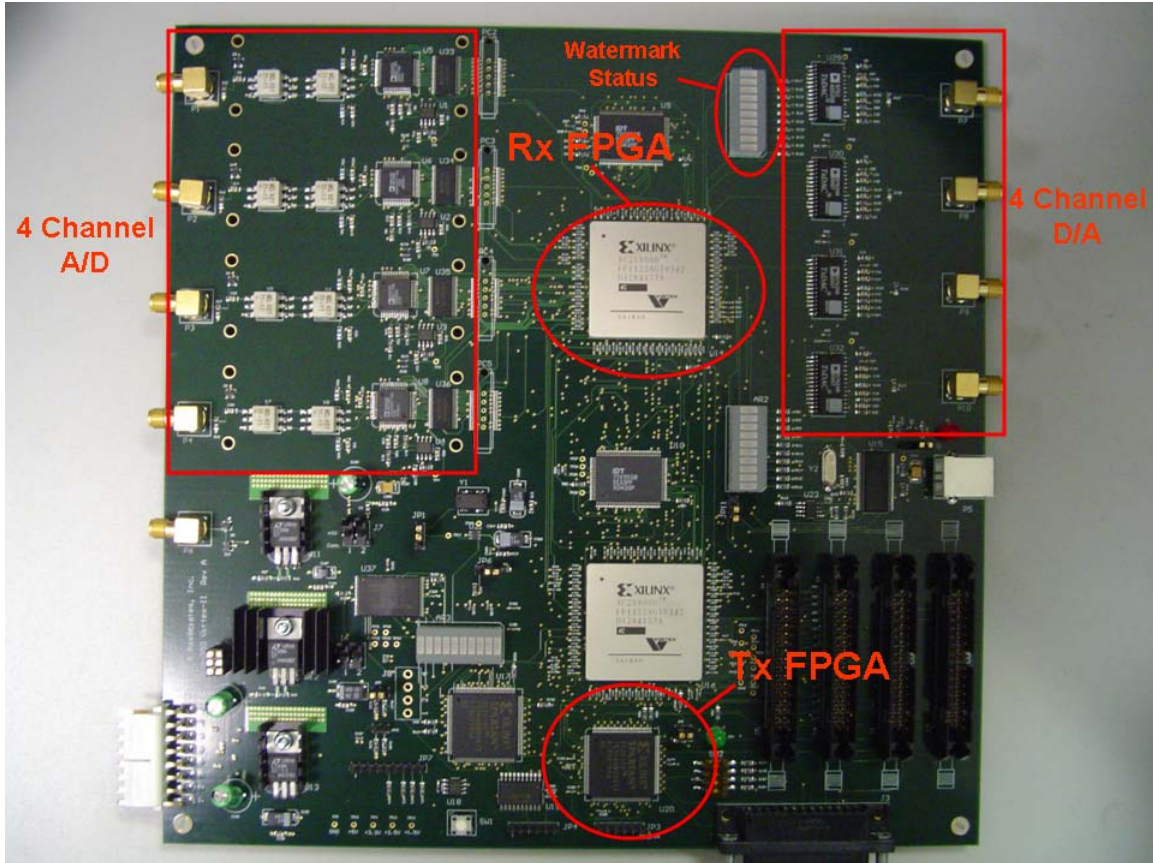

Figure 2.3-2: GVA-350 FPGA Board.

This photo of the GVA-350 shows A/D and D/A sections, as well as transmit and receive FPGAs. A ten segment LED display is used for watermark detection status.

3. Watermark System Design

A simplified block diagram of the overall system design can be seen in figure 3.0-1. A simplex, or 'one way' system was developed for proof-of-concept. As stated earlier, the modulation format chosen for this design was Offset Quadra-Phase Shift Keying. Radio Frequency Integrated Circuits (RFICs) from RF Micro Devices [3] were employed due to low cost, high performance, small footprint, and ease of implementation. Coaxial cable

was used to prevent RF emissions during testing, thus a simple 'attenuation' and additive white noise channel was employed for this initial phase of testing. Data for the system was supplied by either a bit error rate monitor, or computer data (images, video, data files, etc.), with a maximum throughput of approximately 350 Kbps.
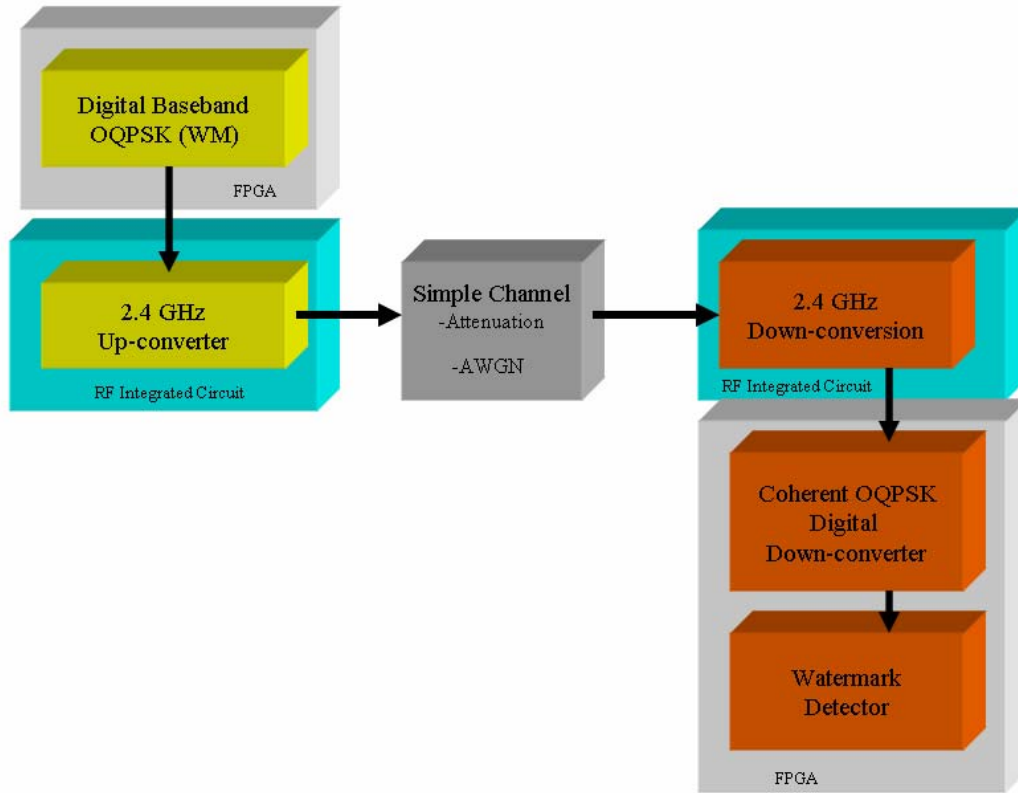

Figure 3.0-1: Simplified Block Diagram.

This simplex system uses FPGAs for baseband processing, including watermarking signature. RFICs are employed for radio frequency functions. Coherent reception is performed digitally, including watermark authentication.

3.1 Transmitter

The transmitter's digital portion can be seen in figure 3.1-1. Data from either a Bit Error Rate (BER) monitor or miniature remote Ethernet Bridge [9] is fed into the transmit FPGA. Obviously, the BER will be used for performance testing. The Ethernet Bridge will be used as part of a video demonstration system. A Xilinx Spartan (XC2S100) FPGA is used to format the data into OQPSK baseband data – producing the In-phase (I) and Quadrature (Q) channels. Each channel is differentially encoded. The final step is to add the watermarking signature. Other functions performed on-chip include: clock

generation (both internal logic and external data), and the option of a 'scrambling code' for operation with 'bursty' Ethernet data. This latter function ensures that a constant bit stream of data is sent to the modulator even during periods of inactive data, which would otherwise cause difficulty for the receiver's phase and frequency tracking loops.
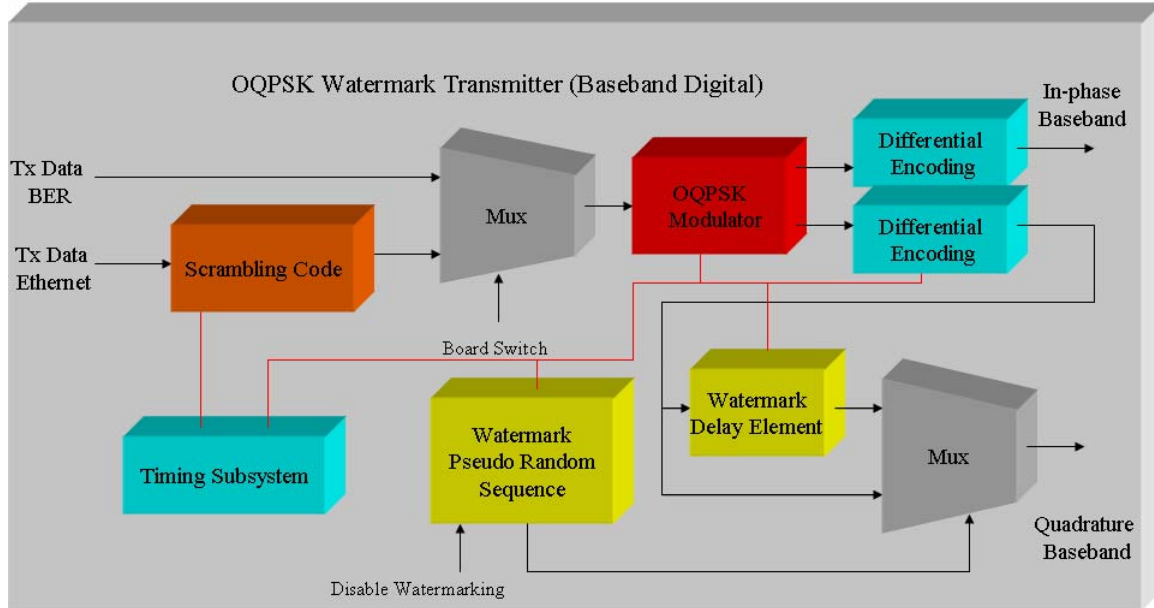

Figure 3.1-1: Transmitter Digital Block Diagram.

This digital portion of the transmitter is implemented in a FPGA. All baseband processing is performed here, including watermark signature, OQPSK modulation, and differential encoding.

The RF portion of the transmitter was simplified by the use of RF Micro Device's RF2422 direct quadrature modulator. This monolithic integrated quadrature modulator is capable of universal direct modulation up to 2.5 GHz. An onboard power amplifier is capable of +3 dBm power output. This RFIC accepts the digital in-phase and quadrature signals directly from the Xilinx Spartan FPGA. An example of a RFIC can be seen in figure 3.1-2.
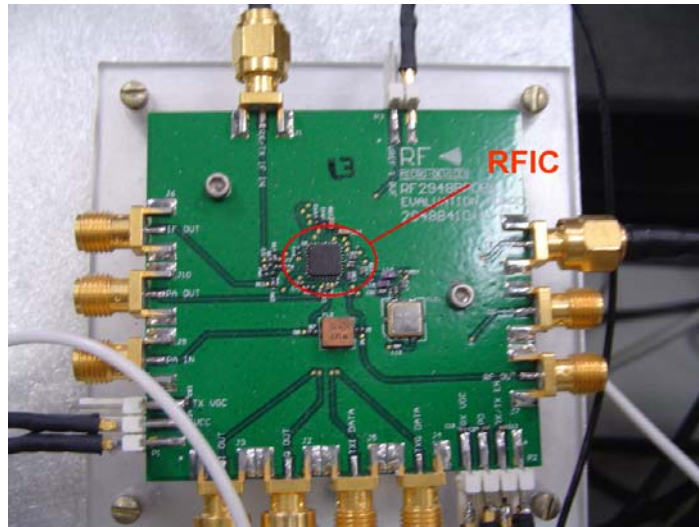
Figure 3.1-2: Radio Frequency Integrated Circuit (RFIC).

The RFIC shown here is the RF Micro Devices 2948 chip (highlighted in red). Various filters and passive components make up the rest of the evaluation board. This board measures approximately 2.25 inches square.

3.1.1 The Watermark Concept

The concept of this watermark signature is very simple; of the two data channels present in the modulated waveform, one of these channels has a bit stream whose period varies, relative to the other channel, in a pseudo random fashion. In-other-words, the data bit transitions (from 1 to 0 or vise versa) do not always begin and end as they normally would. This is accomplished by adding a pseudo random timing offset to the quadrature channel. The quadrature channel symbols are either transmitted in the standard fashion (if the watermark pseudo random code equals "0"), or 'shifted' by 12.5 percent relative to the in-phase symbols (if the watermark pseudo random code equals "1"). The idea here is that this 'timing jitter', as one could call it, does not noticeably affect performance of the waveform, and is not readily noticeable to an observer that is not specifically looking for it - yet can be seen by those who know what to look for.
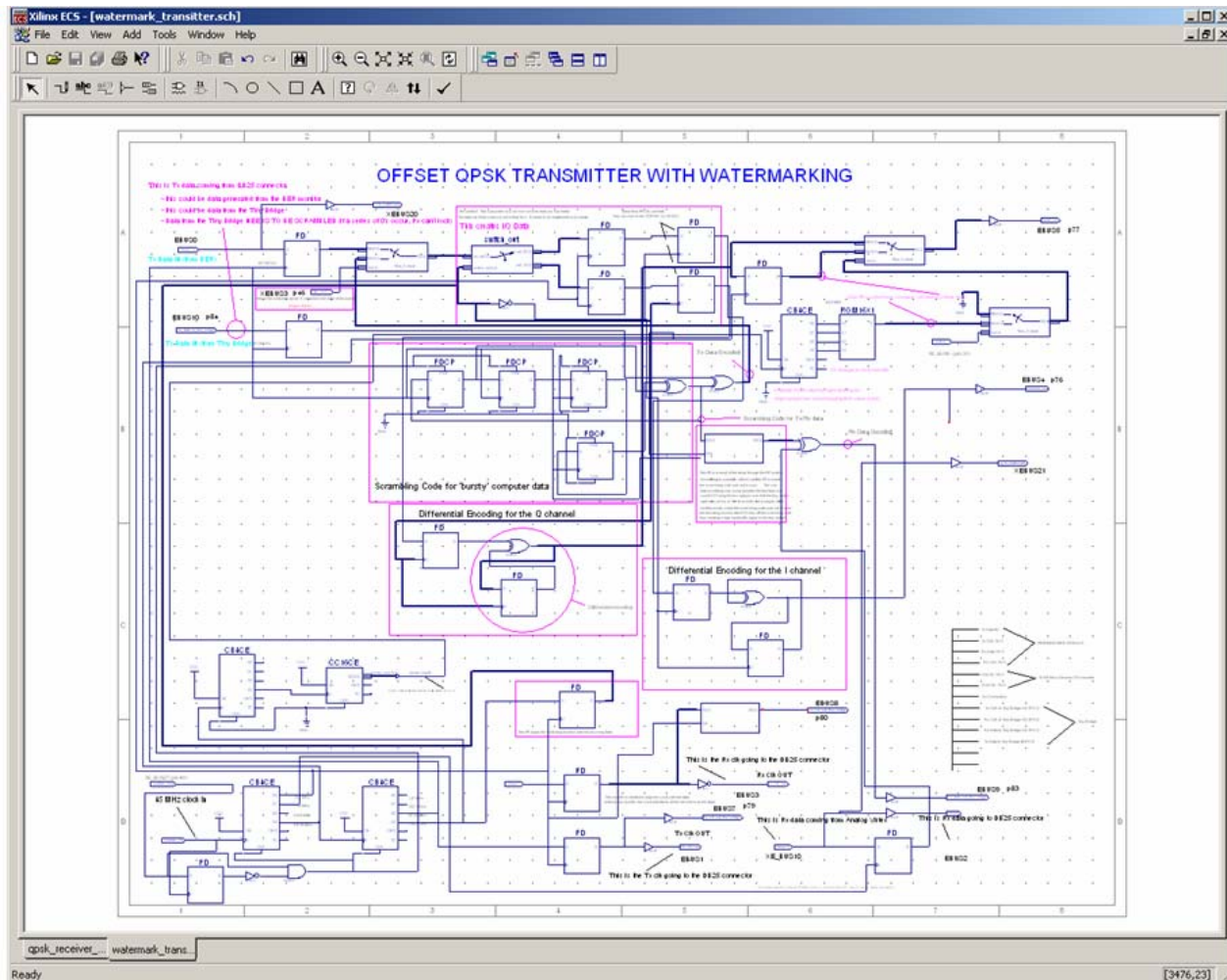
Figure 3.1-3: Transmitter Digital Schematic Diagram.

The OQPSK Watermark transmitter was designed using the Xilinx Engineering Capture System (ECS). A Xilinx Spartan FPGA was used for implementation (XC2S100).

The watermark pseudo random code is placed in a Read Only Memory (ROM) and sequenced using a counter. In the current configuration, which is subject to change, the PN code is 16 chips long, and each chip in this pseudo random sequence corresponds to 128 data symbols. Figure 3.1-3 displays the actual Xilinx ECS top-level schematic diagram.

3.2 Receiver

A detailed block diagram of the receiver can be seen in figure 3.2-1. Two RF Micro Device's RFICs handle the down conversion process to a very low Intermediate Frequency (IF) of approximately 1.9 MHz. These chips were intended to be used for full down conversion; i.e., resulting in baseband I and Q data. Full demodulation by this chip set would not allow for watermark authentication; thus, it was decided to use these RFICs to down convert to 1.9 MHz, and then perform the final coherent demodulation process digitally within the FPGA.

The first RFIC, the RF2494, is a monolithic (Si Bi_CMOS) integrated receiver front end suitable for 2.4 GHz Industrial/Scientific/Medical (ISM) band applications. It contains a low-noise amplifier (LNA), a double balanced mixer, and a second RF amplifier. The bandpass filtering, shown in figure 3.2-1, is actually performed off-chip by a Surface Acoustic Wave (SAW) filter. The Local Oscillator (LO) is also provided off-chip; in this case, a programmable frequency synthesizer was used.

The Intermediate Frequency (IF) signal output by this chip is centered at 374 MHz. This signal is then filtered by a SAW Bandpass Filter (BPF) before being input to the RF 2948 'IF quad' demodulator. A constant gain (15 dB) amplifier is the first function within the RF 2948. The single-ended input to this filter is converted to differential, and stays differential until the final stage of this chip where it is converted back to single ended. There are a series variable gain amplifiers, producing gain anywhere from 4 to 70 dB. The signal is then sent to a double-balanced differential mixer. The LO for these mixers is again provided off-chip by a programmable frequency synthesizer. The chip provides a 90 degree phase shifter for I/Q baseband demodulation; but, again, this is not taken advantage of. Instead, the output of one of the rails (in-phase), after being bandpass filtered and centered around 1.9 MHz, is sent to the GVA-350 for digitization and final down conversion.
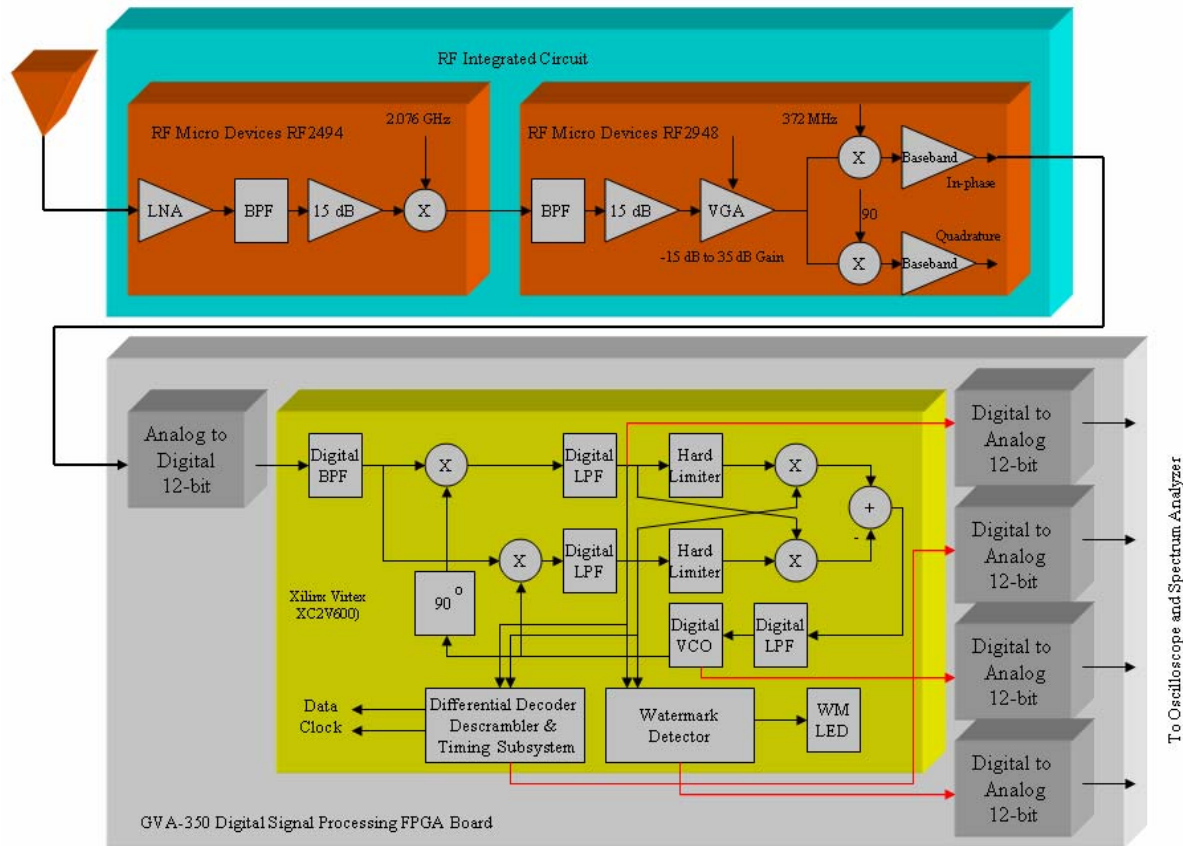
Figure 3.2-1: Receiver Block Diagram.

The receiver uses a '2 chip' solution from RF Micro Devices for the analog section. The final down conversion is performed digitally using a Xilinx Virtex FPGA. 'Costas Loop' architecture provides phase and frequency tracking.

The GVA-350 utilizes 4 Analog Device's AD9432 100 MSPS 12-bit A/D converters. 100 MSPS is the maximum sample rate of these A/D converters. The GVA-350 routes a separate I/O pin to each A/D (and D/A) clock input so that the FPGA can precisely clock each of the I/O channels with identical or different rates. In this case, a 45 MHz clock was used for the A/Ds and D/As, resulting in 45 MSPS (12-bits per sample) data stream from each of the four analog input channels being fed to the Virtex FPGA.

Although the watermark detection subsystem was the focus of this receiver design, a surprising amount of time and effort was needed to develop a coherent OQPSK receiver. It was also surprising that many textbooks and web-based tech notes varied noticeably on receiver design "details" or many simply lacked the details altogether. After some trial and error, and consulting experienced colleagues, the 'Costas Loop' [5] was chosen for the basic receiver architecture. The Costas Loop refers to an architecture which allows

the receiver to perform phase and frequency tracking of the suppressed carrier OQPSK waveform; thus producing the baseband I and Q channels. The Costas Loop architecture requires the use of a Voltage Controlled Oscillator (VCO). For FPGA implementation, a Direct Digital Synthesizer (DDS) is used as part of the VCO. The DDS is offered as an Intellectual Property core from Xilinx, and can be tailored to a wide variety of applications using the Xilinx Logicore software interface.

Several band-pass filters were needed in the receiver design and were developed using a combination of SPW and Xilinx ISE. SPW offers a tool called FDS, or Filter Design System, which is an easy to use software tool for the design of lowpass, bandpass, highpass and stopband filters. FDS allows the user to specify filter parameters, such as cutoff frequency, passband frequency, passband and stopband ripple, type of filter, etc. FDS will then calculate several options for the user, using different filtering algorithms such as Butterworth, Chebyshev, etc., and will provide the user with the filter coefficients for each design, along with the associated graphs, such as the frequency magnitude and phase response. From here, the filter coefficients are used in a Distributed Arithmetic (DA) Finite Impulse Response (FIR) filter, which is a Xilinx IP core. The IP core creates an optimized FPGA implementation of the filter based upon the user's coefficients, along with several other user selectable parameters via the software GUI.

The actual schematic of the receiver's digital portion can be seen in figure 3.2-2. Within the diagram, one can see a timing subsystem and watermark detection subsystem. These designs are contained on separate schematics, and will be discussed subsequently.

Figure 3.2-2: Receiver's Digital Schematic Block Diagram.

The receiver's digital section contains the Costas Loop receiver, timing subsystem, and watermarking detection subsystem. The later two are held in separate schematics, thus allowing for a more 'viewable' schematic.

The watermark detection subsystem block diagram can be seen in figure 3.2-3. The objective of this detection system is simple: observe the zero crossings of the in-phase and quadrature channels to see if a pseudo random sequence has been embedded in their relative difference.

The process starts by aligning the two OQPSK channels; this was accomplished by a ½ symbol delay in the in-phase channel. Each channel is then converted to a pulse stream where each pulse represents a zero crossing of the waveform. An accumulator looks for (counts) the number of times a zero crossing occurs in a specified region; i.e., has a 'watermark' phase advance occurred? The timing signal used by the accumulator was critical; it had to account for inaccuracies and noise present in the system, yet try to

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minimize false readings. The initial (calculated) timing signal was modified after some experimentation. A 15-tap lowpass filter was developed using the Xilinx Distributed Arithmetic FIR filter intellectual property core. Figure 4.0-14. shows the output of the accumulator (bottom waveform) and the lowpass filtered result.
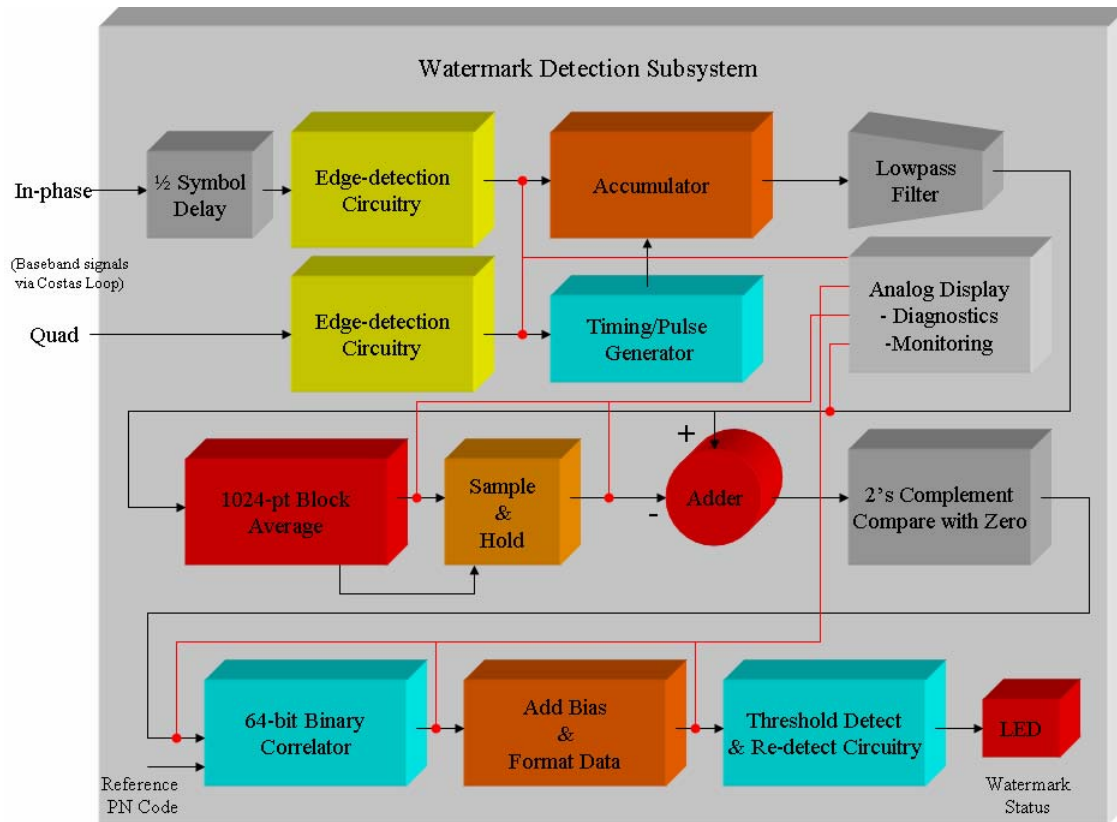
Figure 3.2-3: Watermark Detection Subsystem.

The watermark detection subsystem, using edge detection, looks for a PN code embedded in the received signal. A correlator compares a reference code with the received code to determine if the watermark is present.

The next step after filtering is to determine if the resulting waveform matched the reference pseudo random sequence; i.e., is the watermark present or simply noise? Actually, there are three possibilities: no watermark present, a watermark is present, but it is not the correct watermark PN sequence, or a watermark is present and is the correct sequence.

A correlation process is used to detect the presence of a watermark and ensure it is the correct PN sequence. A Xilinx IP core (bit correlator) is used for the matching process between the received sequence and the reference sequence. The bit correlator does a bit-by-bit comparison between a user defined bit pattern and the input data, producing an

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unsigned output proportional to the number of matches. As stated earlier, the PN code is 16 chips long, but 4 samples are used for every chip; thus, a 64-bit correlator was used. The signal that is produced by the accumulator/lowpass filter is a 16-bit discrete signal (a sampled analog waveform, with each sample represented by 16-bits), not a binary signal. Therefore, in order to use the bit correlator, the input waveform had to be converted to binary waveform. A '2's complement compare with zero' function was used after the waveform's mean value was subtracted. The output of the correlator, after some minor formatting alterations, is compared to a threshold. A value above this threshold means the 'correct' watermark is present. The threshold was experimentally adjusted after testing under various conditions; i.e., differing noise levels. A ten segment LED display on the GVA-350 flashes to notify the user that a watermarked signal was detected. After detection, this subsystem constantly processes the received waveform to ensure that the watermark signature is still present.
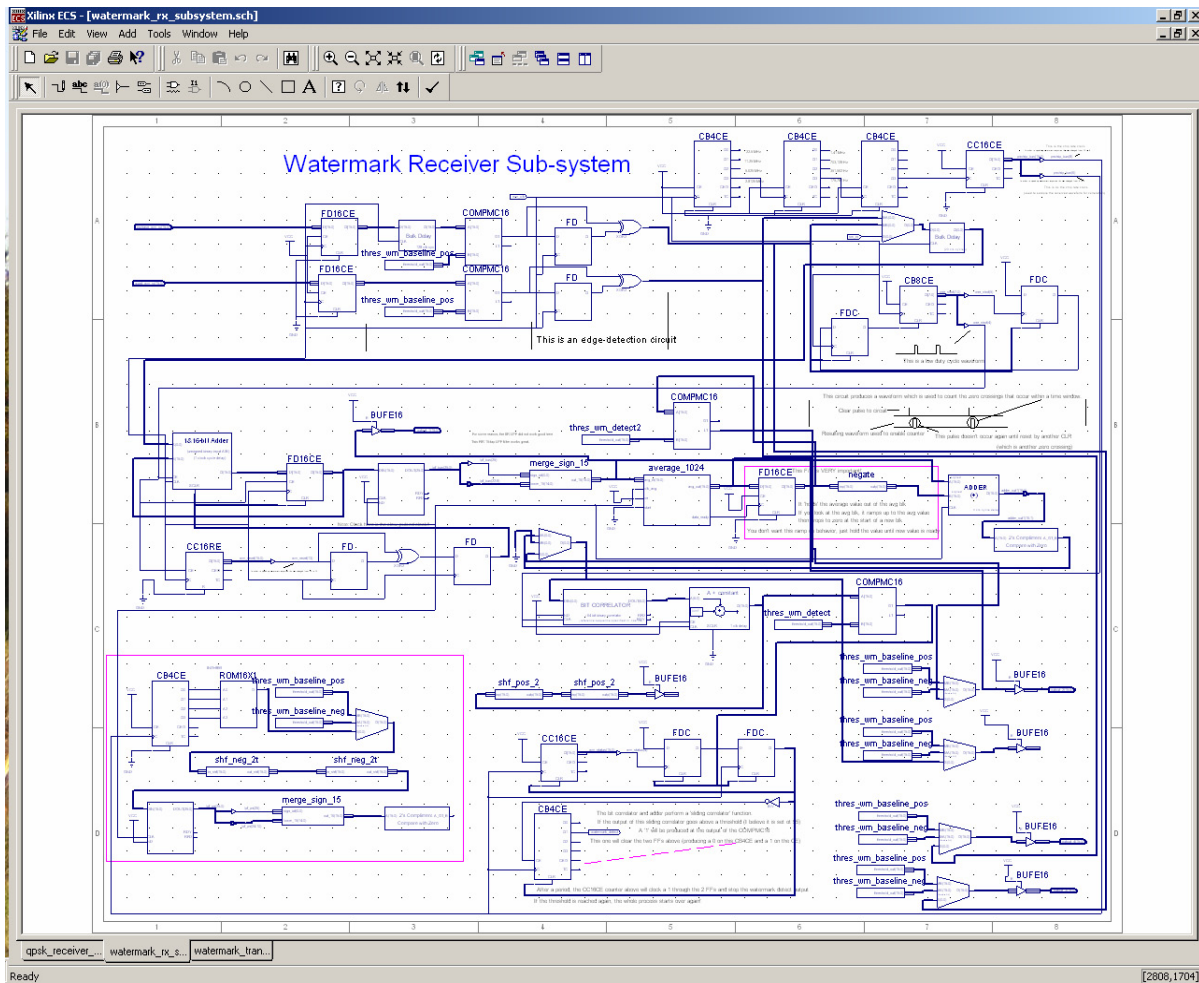
Figure 3.2-4: Watermark Detection Subsystem Schematic Block Diagram.
The watermark detection subsystem shown here uses several Xilinx IP cores, such as the 64-bit binary correlator. 5 Signals are routed from here to the top-level schematic; 4 diagnostic signals and the 'watermark detect' signal.

4. Test Results

Figures 4.0-1 through 4.0-19 display various signals of interest, for example, the spectrum of the RF waveform, or the output of the DDS. The majority of these signals exist within the FPGA as 'discrete time' signals, with amplitudes ranging from binary up to 32-bit. These signals were formatted for use with the GVA-350s 12-bit D/A converters and then displayed on an Agilent 54622D oscilloscope. There are several frequency plots taken from a Hewlett Packard 8562A Spectrum Analyzer. Figure 4.0-20 is a plot of the bit error rate (with and without watermarking) vs. various levels of channel attenuation – which demonstrates the robustness of this watermarking technique. Each figure is accompanied by a brief explanation.
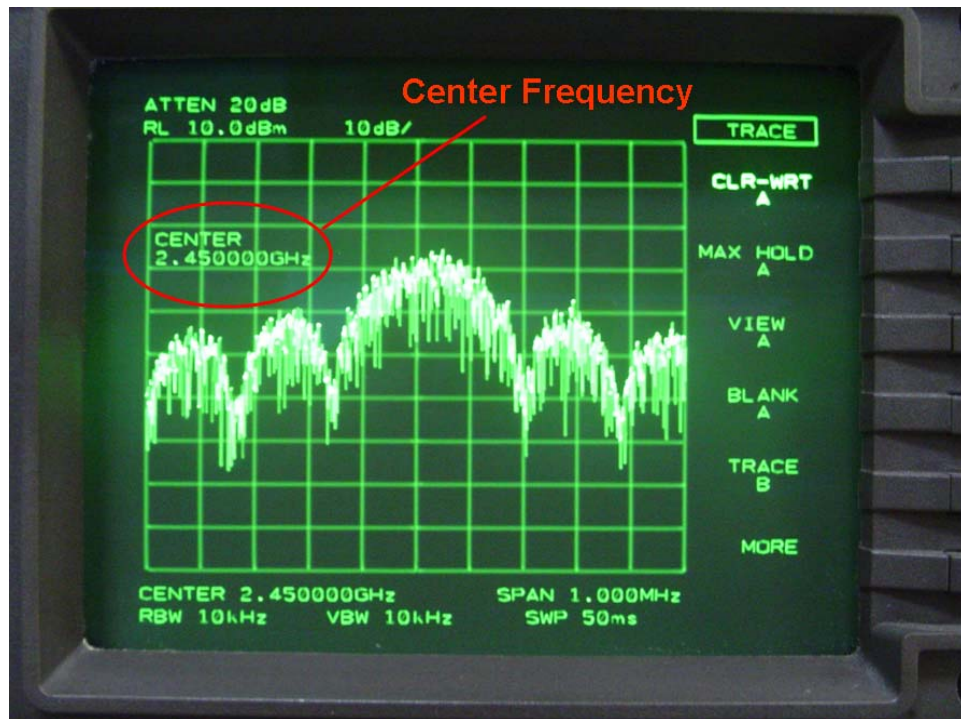
Figure 4.0-1: RF Spectrum.

This spectrum analyzer plot shows the OQPSK signal centered at 2.45 GHz; a portion of the ISM band. RF Micro Device's RF2422 direct quadrature modulator is capable of universal direct modulation up to 2.5 GHz. An onboard power amplifier is capable of +3 dBm power output.
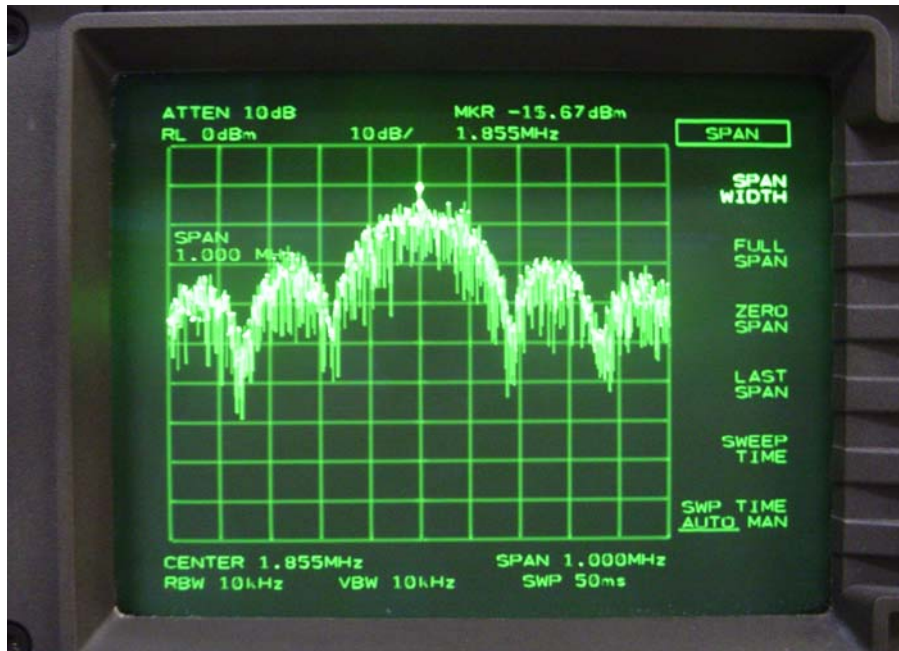
Figure 4.0-2: Received OQPSK Spectrum.

This spectrum analyzer plot shows the OQPSK signal centered at 1.855 MHz. This 'low IF' signal is fully demodulated within the receive FPGA (Xilinx Virtex-II 6000).
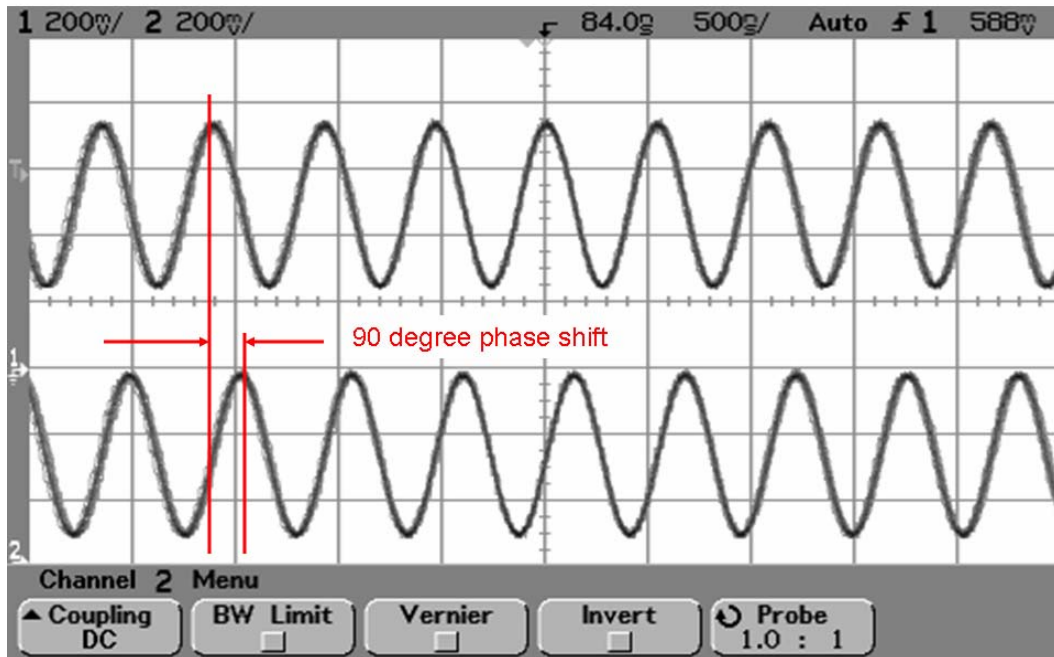
Figure 4.0-3: Direct Digital Synthesizer (DDS) Output.

These DDS signals (in both sine and cosine form) are used to demodulate the received OQPSK signal. Output frequency, DDS clock rate, spurious free dynamic range, and frequency resolution are all parameters of the Xilinx IP core GUI.
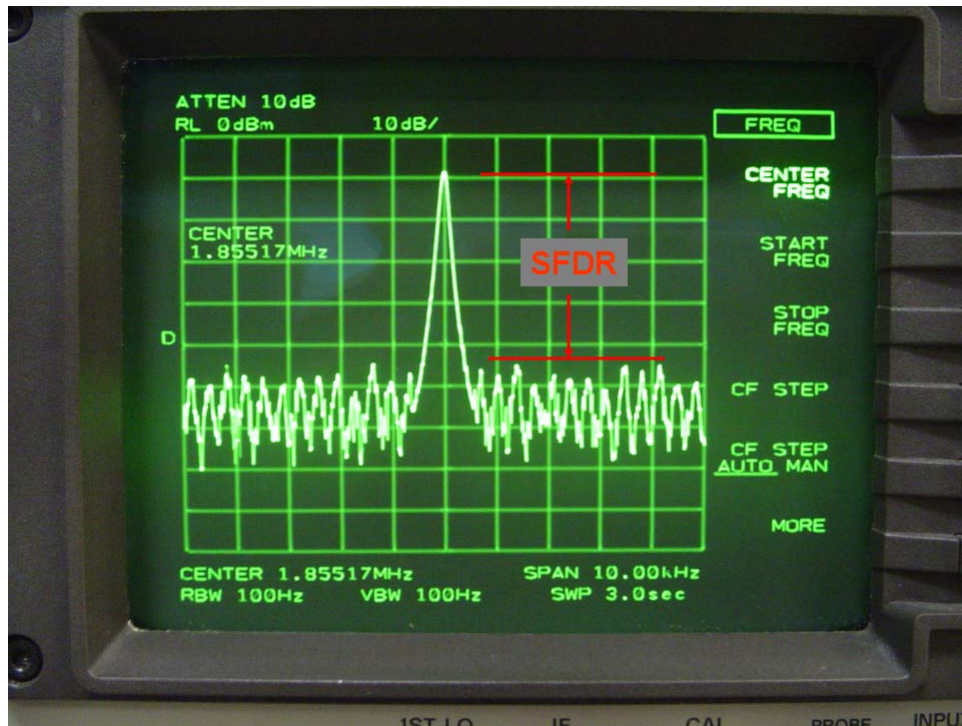
Figure 4.0-4: DDS Output - Spectrum Analyzer.

This spectrum analyzer plot shows how well the DDS signal performs; nearly 50 dB Spurious Free Dynamic Range (SFDR).
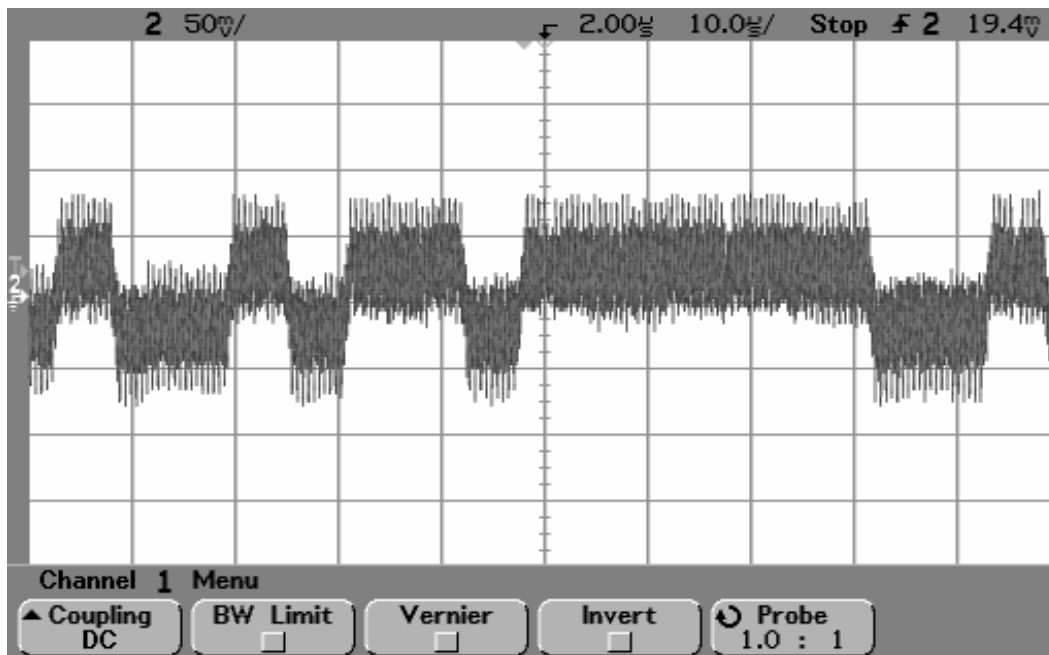
Figure 4.0-5: OQPSK Multiplier Output.

Both the baseband waveform and a carrier component are present in this waveform,
which is the result of multiplying the received signal and the DDS Local Oscillator (LO).
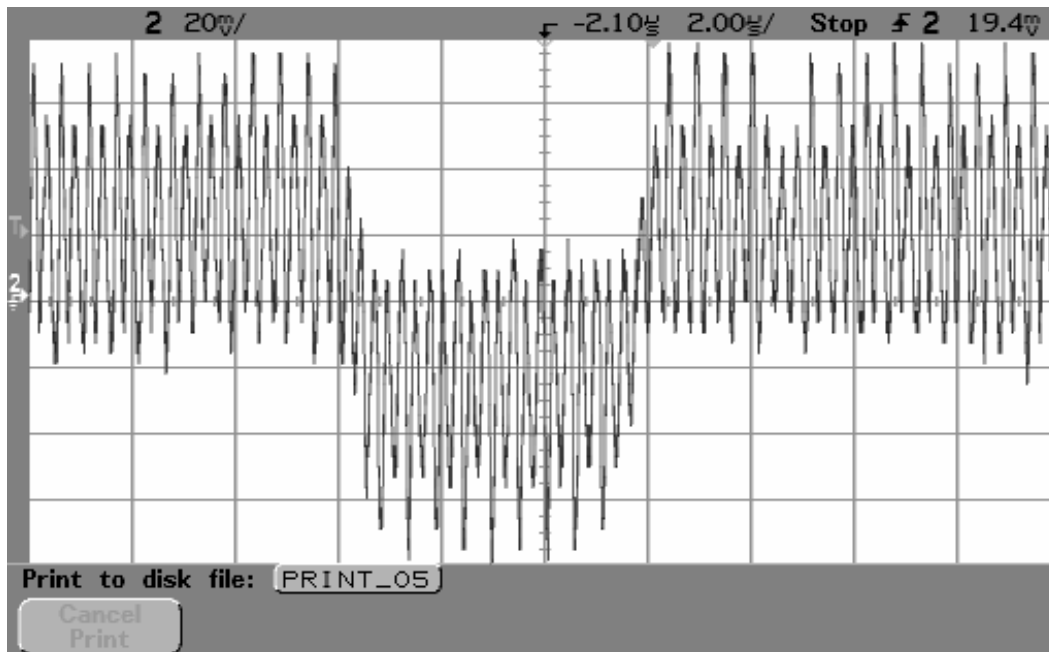
Figure 4.0-6: OQPSK Multiplier Output (zoomed).

This is the same output as the previous figure except the time scale was shortened in
order to better display the carrier component.
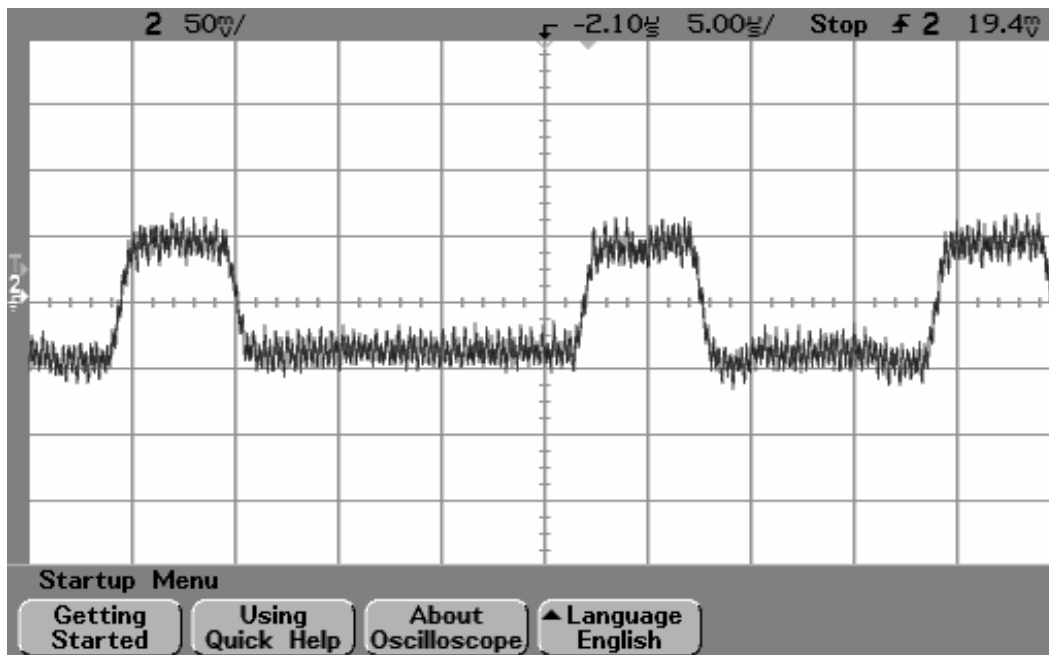
Figure 4.0-7: Baseband Received Signal.

As a result of lowpass filtering, the carrier component (seen in the two previous figures) has been removed.
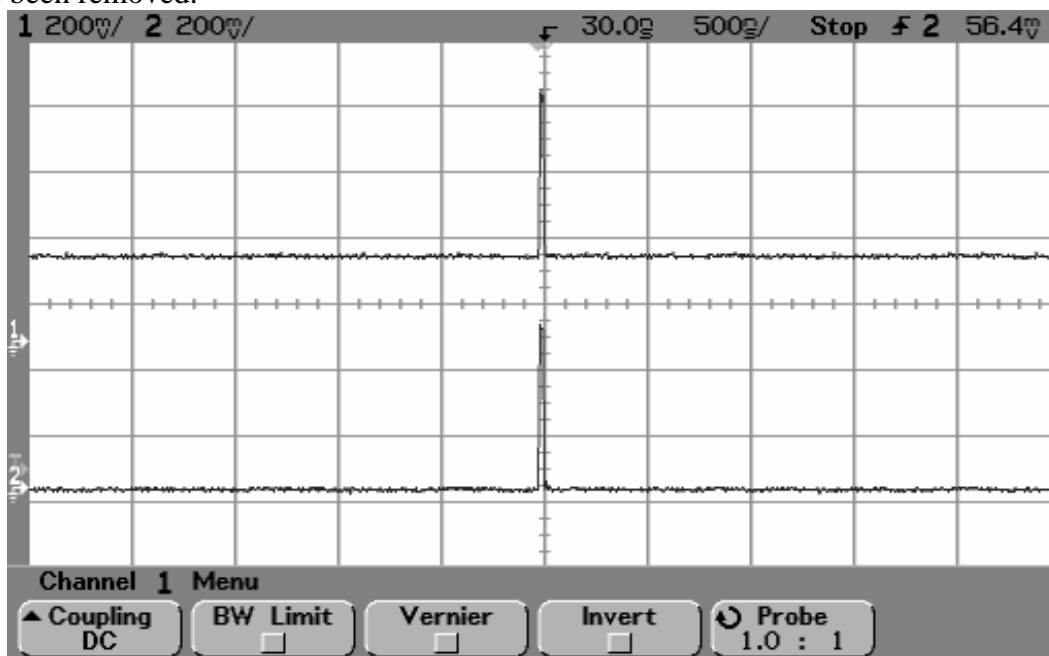
Figure 4.0-8: I/Q Edge Detection Pulses.

The WDS monitors bit transitions and outputs pulses for each transition. In this example, a watermark is not present or a watermark "0" symbol is being transmitted; in either case, the bit transitions occur at the same time.
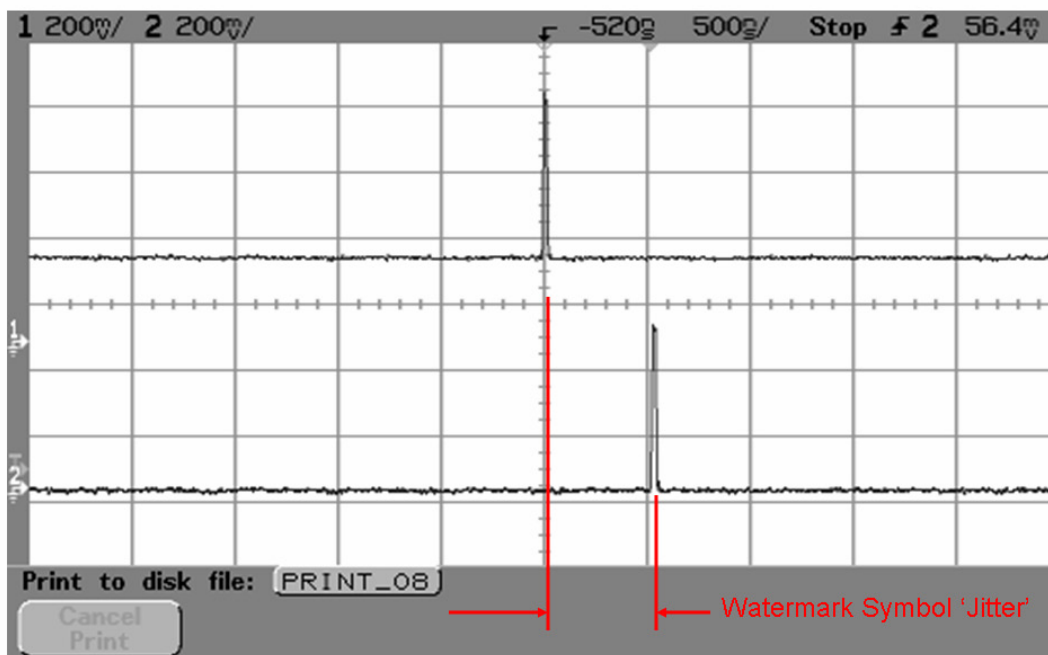
Figure 4.0-9: I/Q Edge Detection Pulses (w/WM).

This is the same signal as the previous figure, except a watermark is present (watermark "1" symbol), thus the bit transitions occur at different times (jitter).
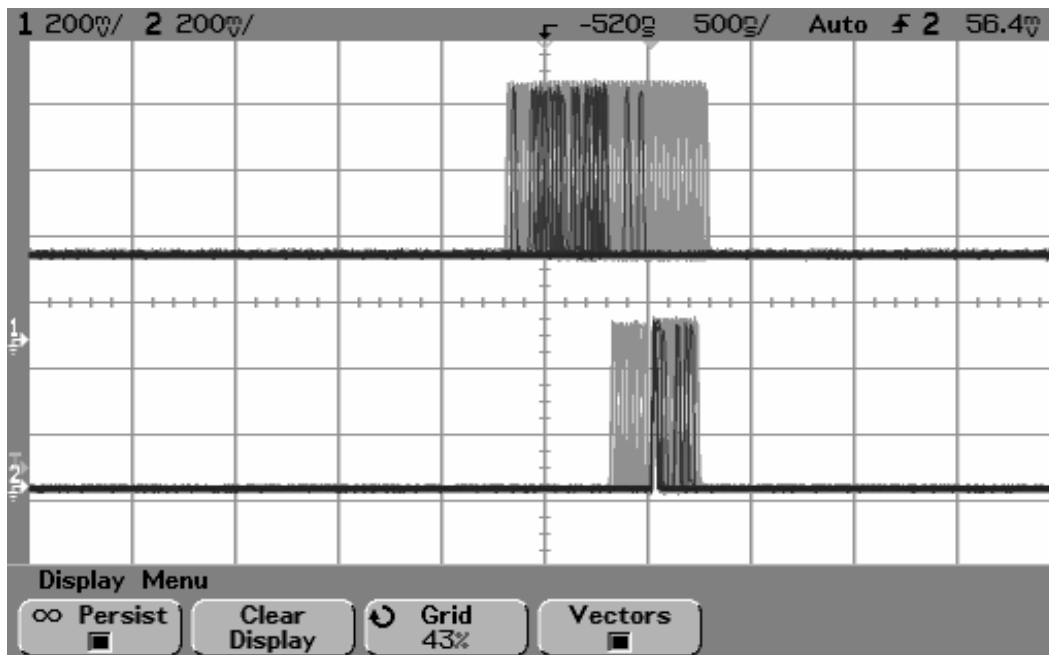
Figure 4.0-10: Multiple I/Q Edge Detection Pulses.

In this figure, the oscilloscope display was set to capture multiple traces. Demodulation inaccuracies and noise can be seen by the wide pulse distribution, yet the watermark detection subsystem was designed to account for this.
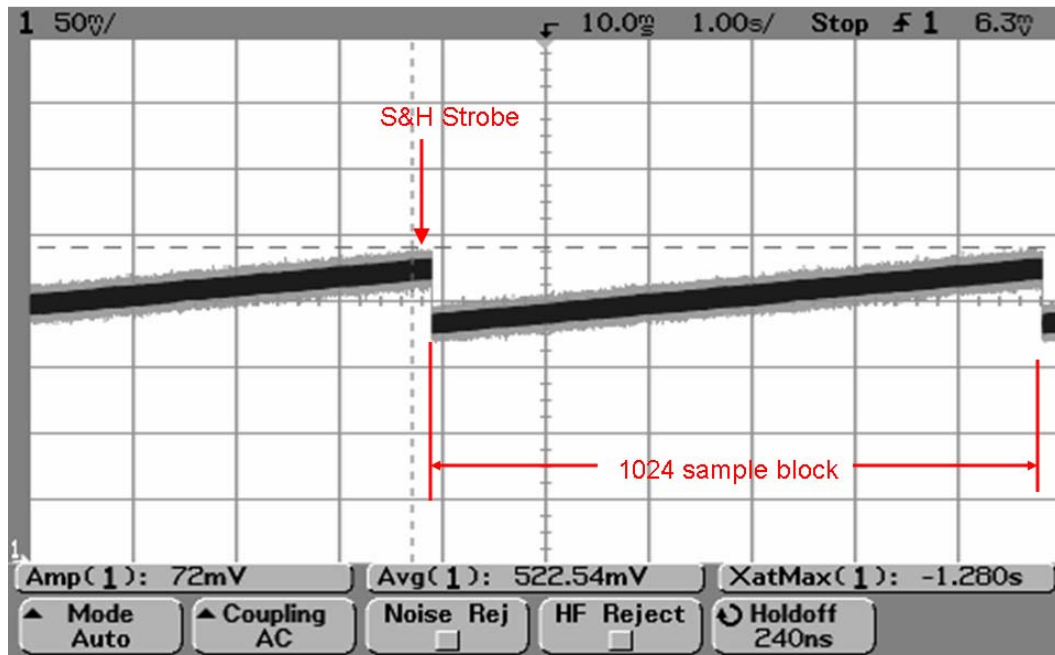
Figure 4.0-11: 1024-pt 'Averaging Block' Output.

Within the WDS, a mean estimator is implemented to remove the DC component of the watermark PN signal prior to correlation. A Sample & Hold (S&H) block samples this output one clock cycle prior to the next block of data.
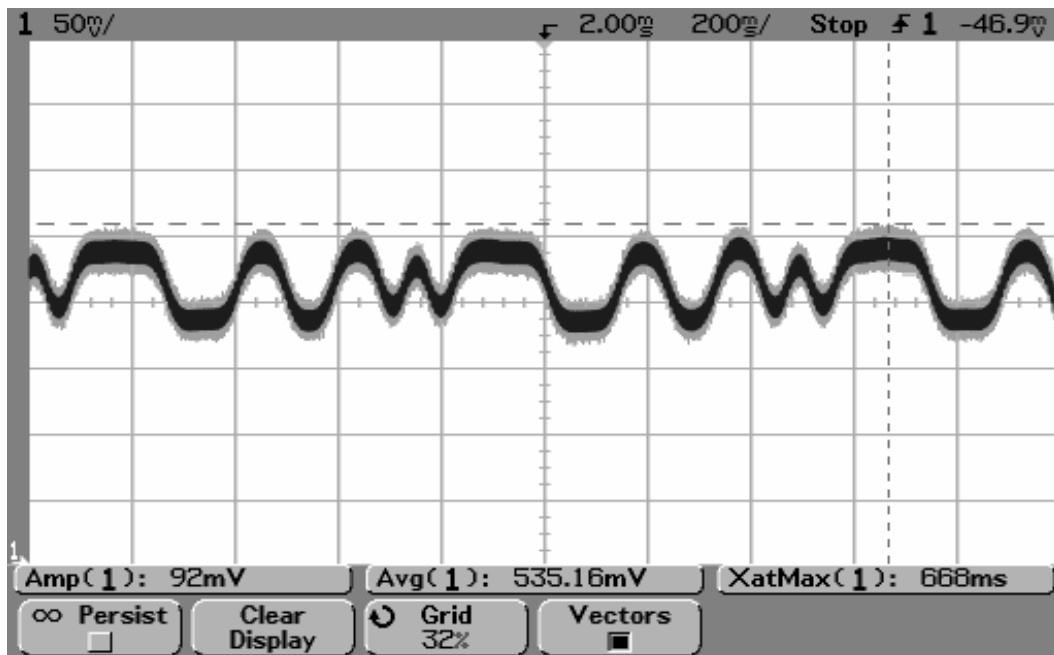
Figure 4.0-12: PN Code derived from Received Waveform's Watermark.

The signal is the result of monitoring pseudo random phase changes in the received waveform. This signal, after some formatting, will be compared with a reference code for authentication.
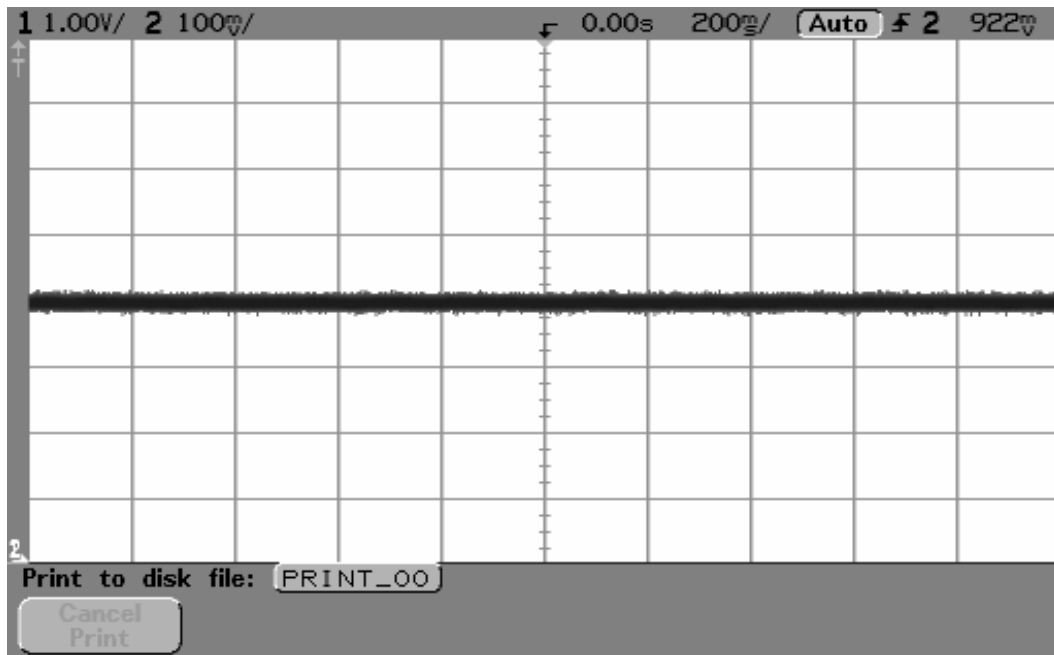
Figure 4.0-13: Output of Watermark Detection Subsystem with Watermark Disabled.

This is the same signal as the previous figure, except that the watermark signature was disabled on the transmitter. As one would expect, no PN code is present.
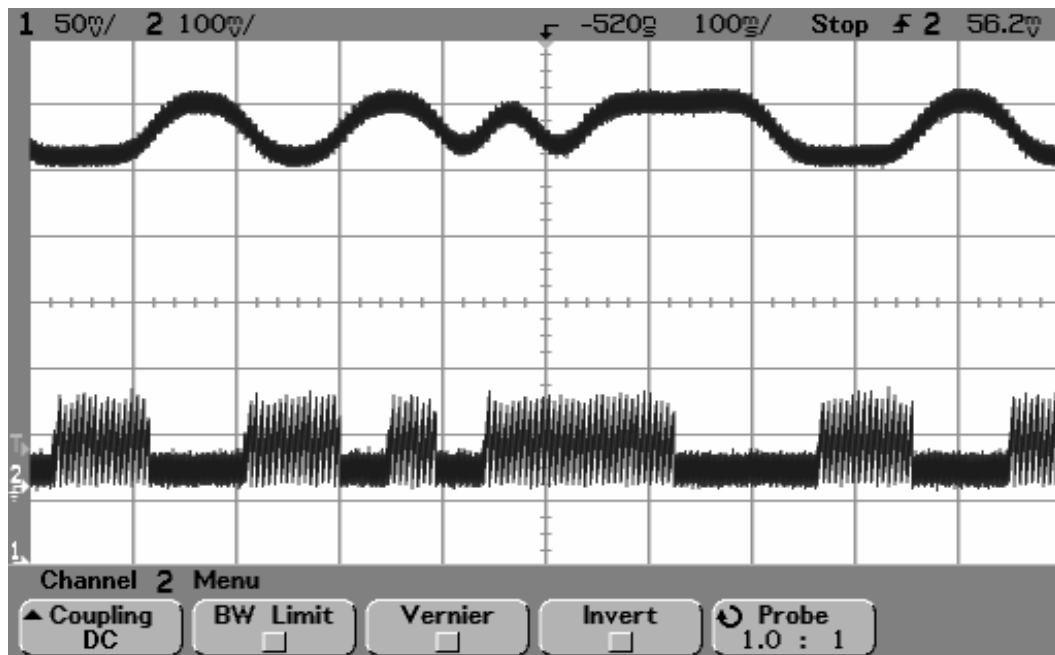
Figure 4.0-14: WDS Accumulator Output.

The lower plot is of the accumulator output, which is counting phase transitions in one of two designated areas (watermark 'zero' or 'one'). This signal is then lowpass filtered (top plot). The filtering process introduces a noticeable delay.
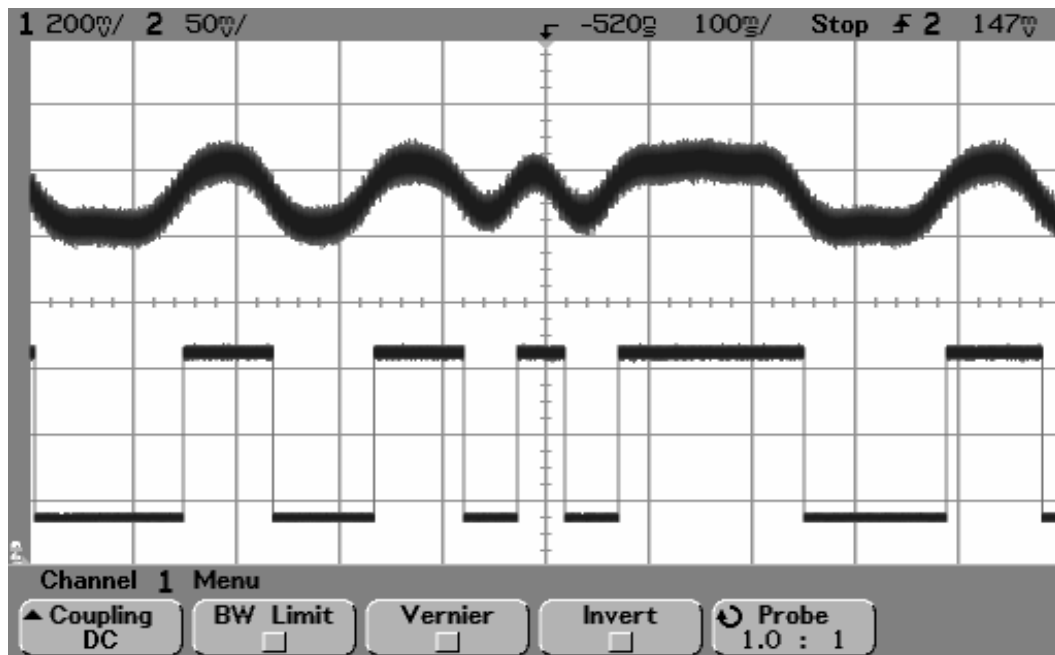
Figure 4.0-15: WDS Received Watermark Estimate.

The top plot is the filtered accumulator output, as in the previous figure.   The lower plot is the output of the '2's complement compare with zero' block - which is a binary waveform. This is then used by the 64-bit correlator for reference matching.
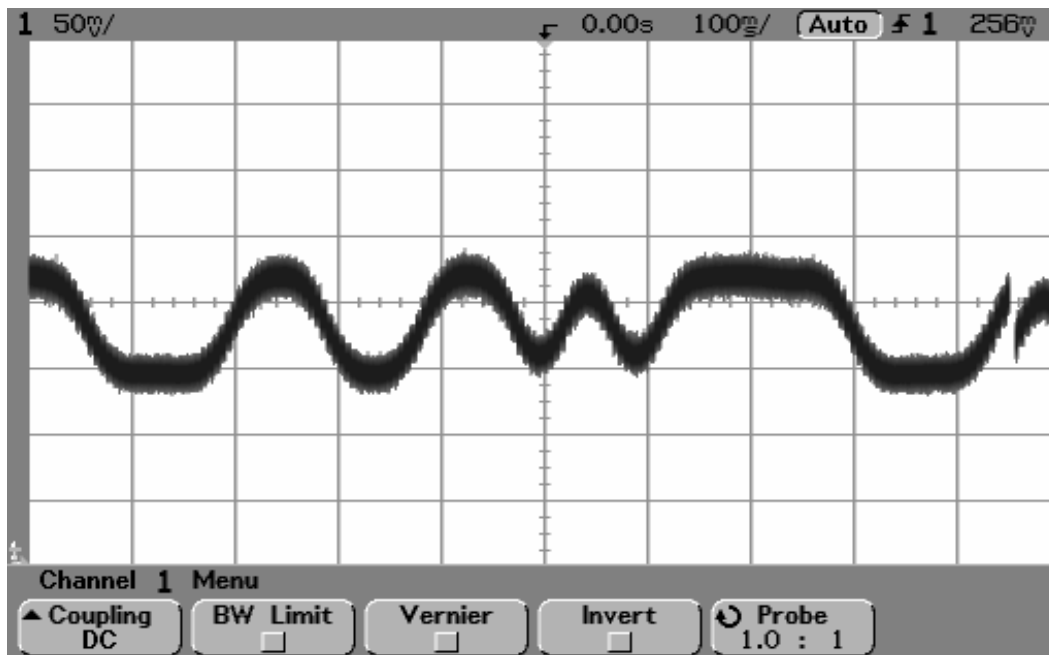
Figure 4.0-16: Watermark PN code with a BER of less than 1e-9.

As one would expect, the watermark PN code is highly distinguishable from channel and receiver noise.
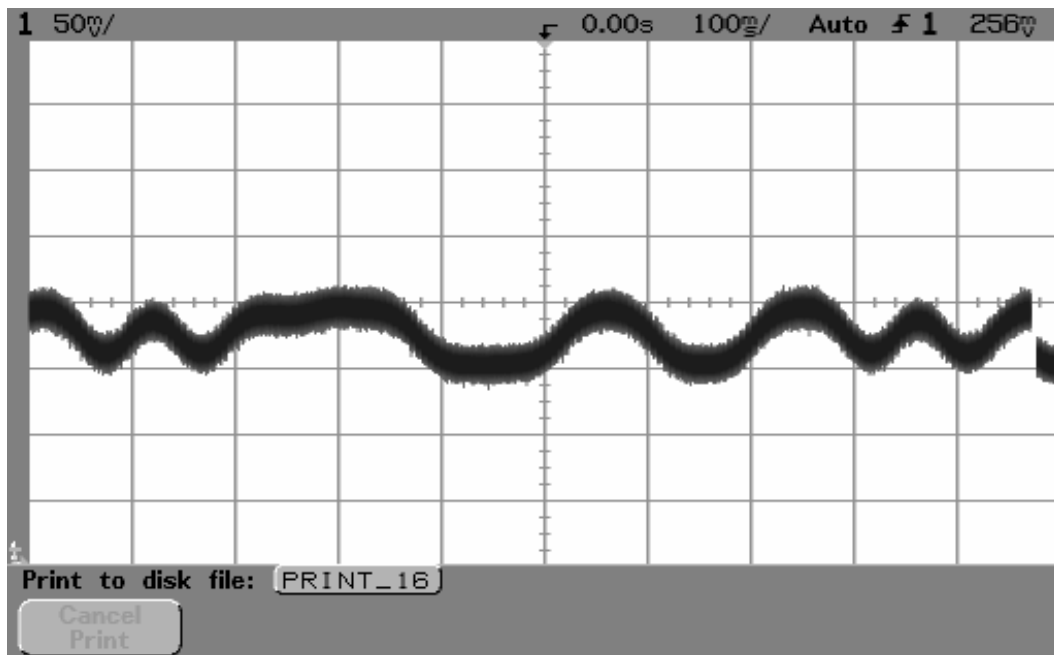
Figure 4.0-17: Watermark PN code with a BER of 7e-3.

The amplitude of the waveform is reduced, but still highly distinguishable from channel and receiver noise.
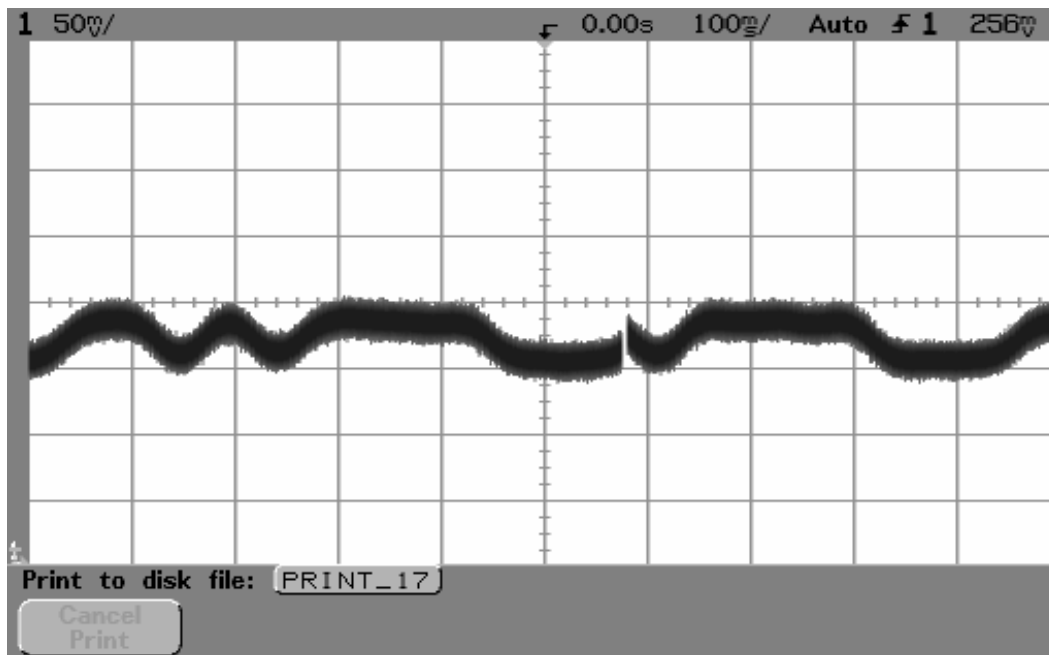
Figure 4.0-18: Watermark PN code with a BER of 8e-2.

The amplitude of the waveform is reduced from the two previous figures, but still distinguishable from channel and receiver noise.
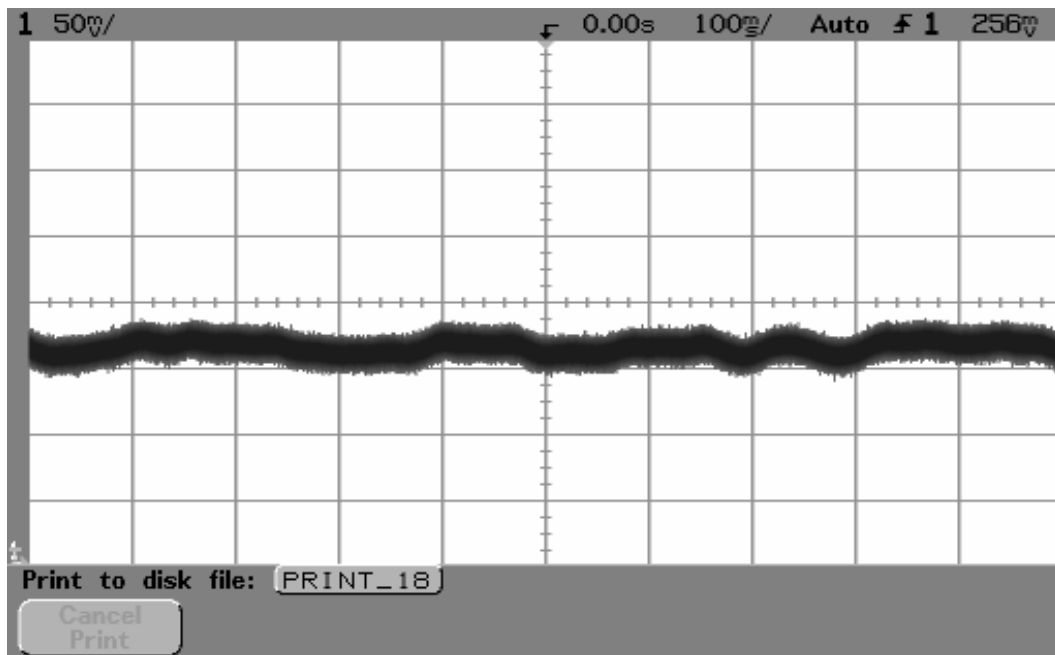
Figure 4.0-19: Watermark PN code with a BER greater than .5e-1.

In this example, the BER is so high that the BER monitor can not achieve synchronization, yet the receiver can still detect the presence of a watermark.
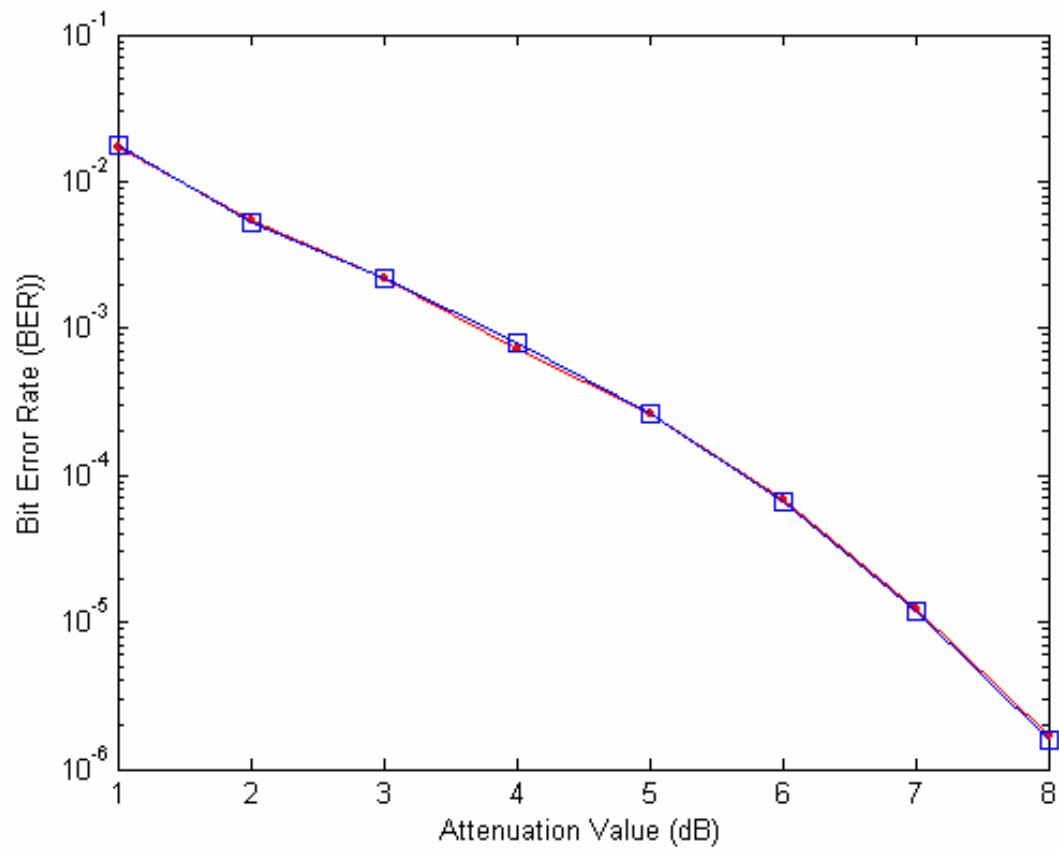
Figure 4.0-20: BER vs. Channel Attenuation.

This is not intended to show absolute, but rather relative, bit error rate performance of the receiver with watermarking enabled/disabled. As one can see, the watermark encoding does not affect BER performance to any meaningful degree. (Data points designated by a square represent watermarking disabled, and points with a dot represent enabled).

5. Conclusions

This is the second project developed using the FPGA rapid prototyping facility; the first being a frequency domain interference excision unit. For this watermarking project, RFICs were added to extend the capability beyond baseband processing, and more accurately model the many problems associated with wireless communication systems. In fact, this is the reason the first watermarking technique proved unsuccessful; the watermark signature was 'lost' in the up and down conversion process. This fact was not revealed in simulation, but during the hardware verification process.

This watermarking technique proved easy to implement, did not seem to affect the 'wireless performance' in any measurable way, and was more robust against noise than the OQPSK waveform itself. Although the technique described in this report used a very simple pseudo-random sequence for watermark authentication, several options are available for added security, if needed. In addition, this watermarking technique is fully compatible with standard quadrature phase waveforms; thus, there would be no compatibility restrictions between mixing watermarking and non-watermarking transmitters and receivers.

6. References

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